FIG. 1
(PRIOR ART)

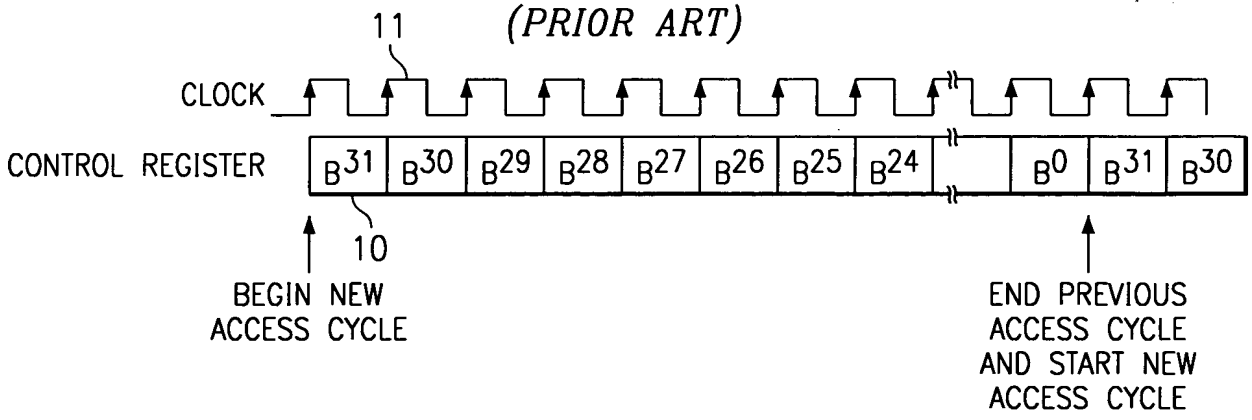
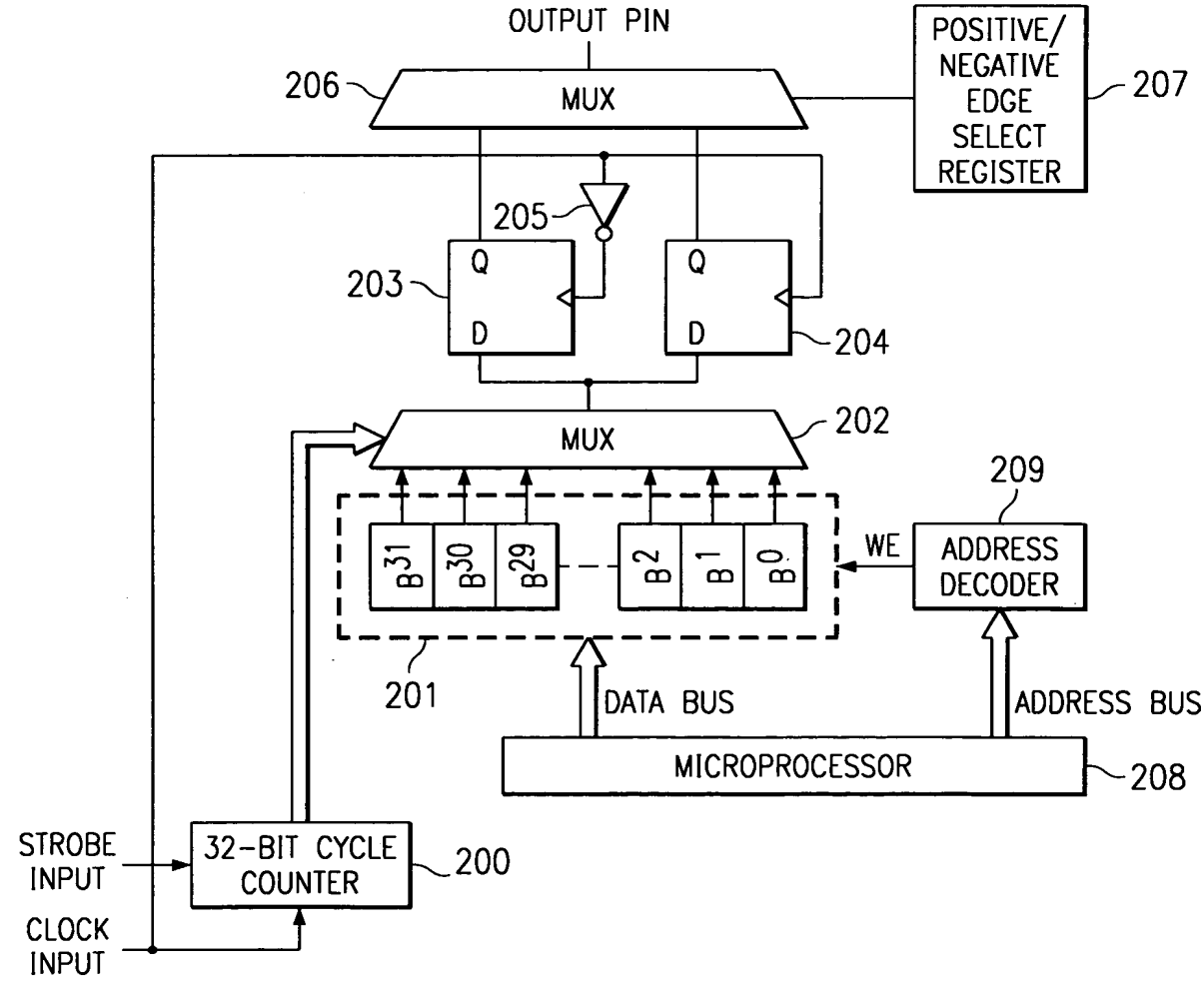


FIG. 2



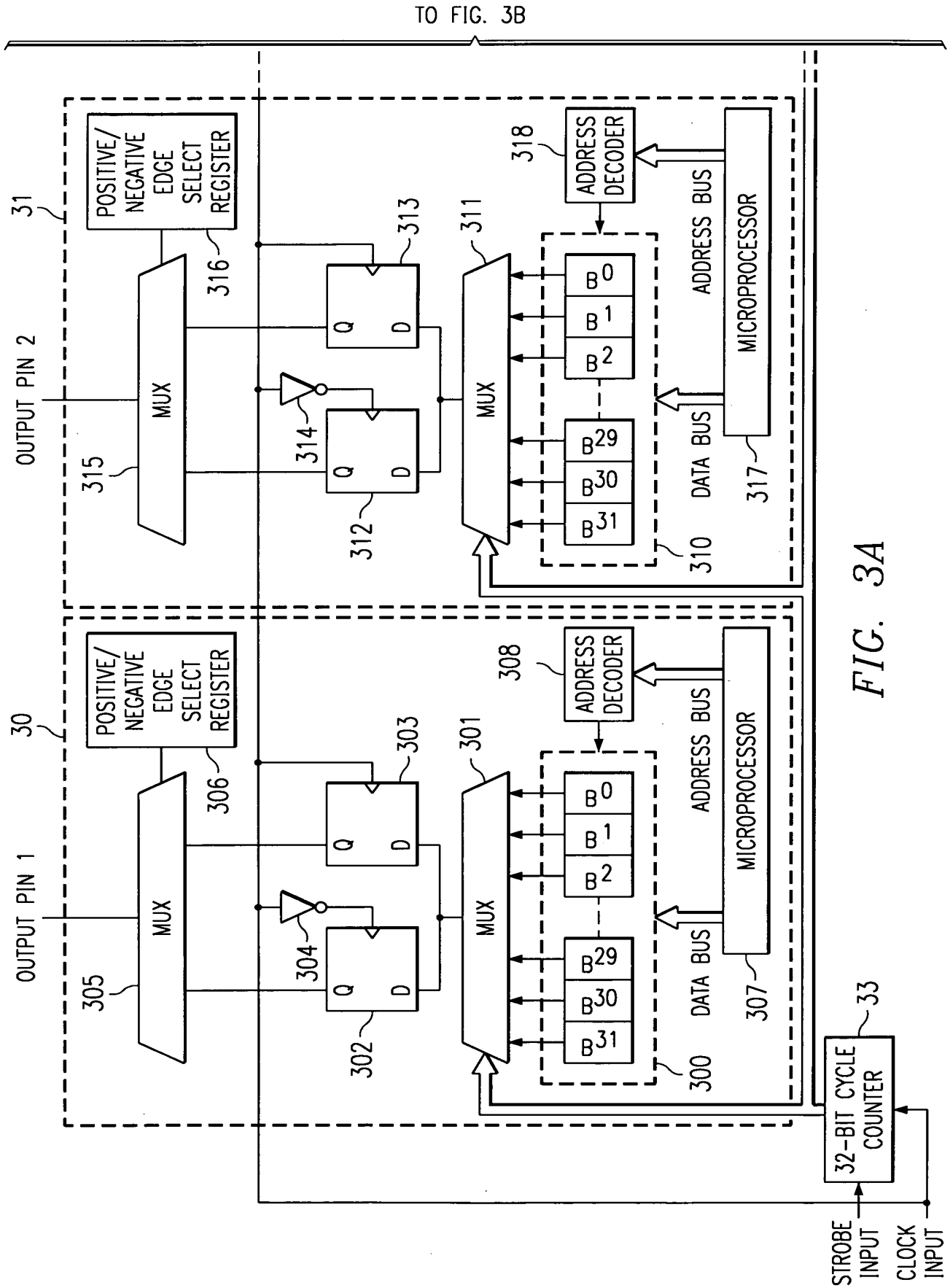
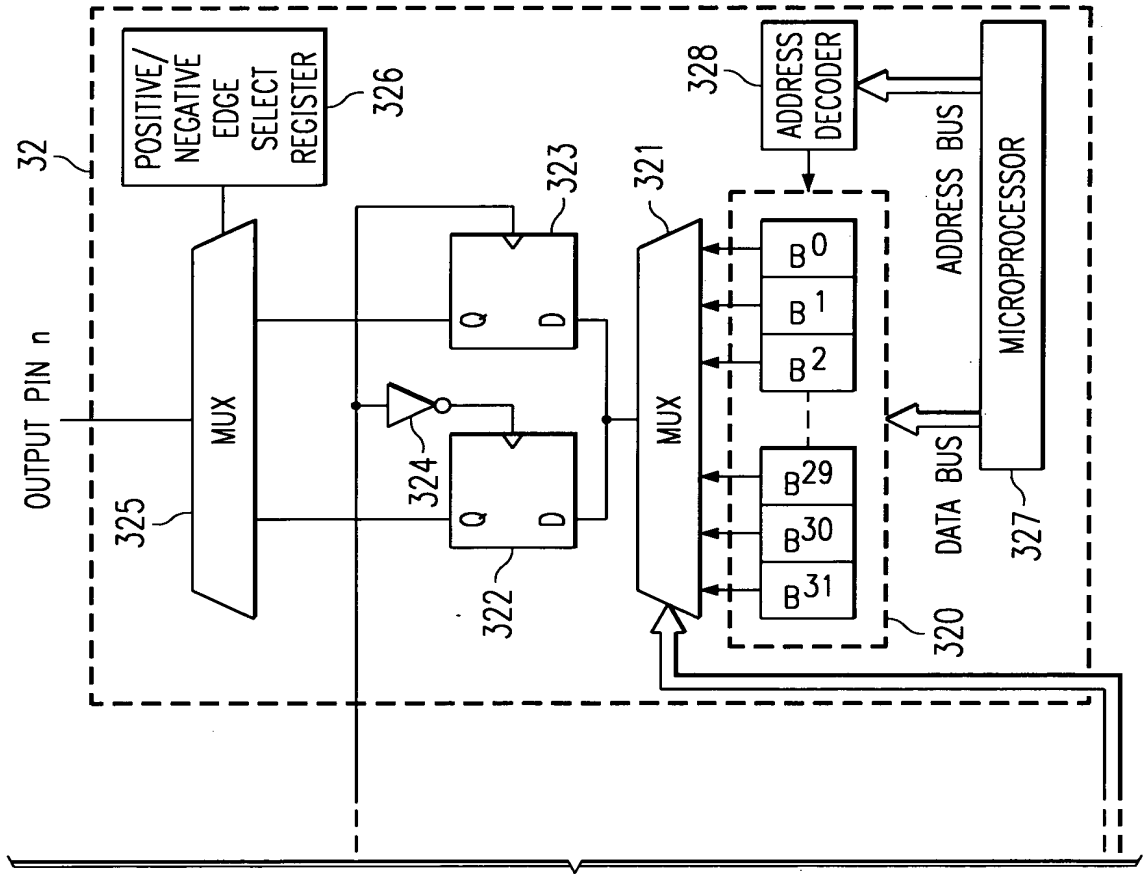

TO FIG. 3B
31
30
OUTPUT PIN 2
OUTPUT PIN 1
POSITIVE/ NEGATIVE EDGE SELECT REGISTER
316
306
MUX
315
305
Q
D
313
303
312
302
314
304
311
301
B0
B1
B2
B29
B30
B31
310
300
ADDRESS DECODER
318
308
ADDRESS BUS
DATA BUS
MICROPROCESSOR
317
307
32-BIT CYCLE COUNTER
33
STROBE INPUT
CLOCK INPUT

FIG. 3A

FIG. 3B



FROM FIG. 3A

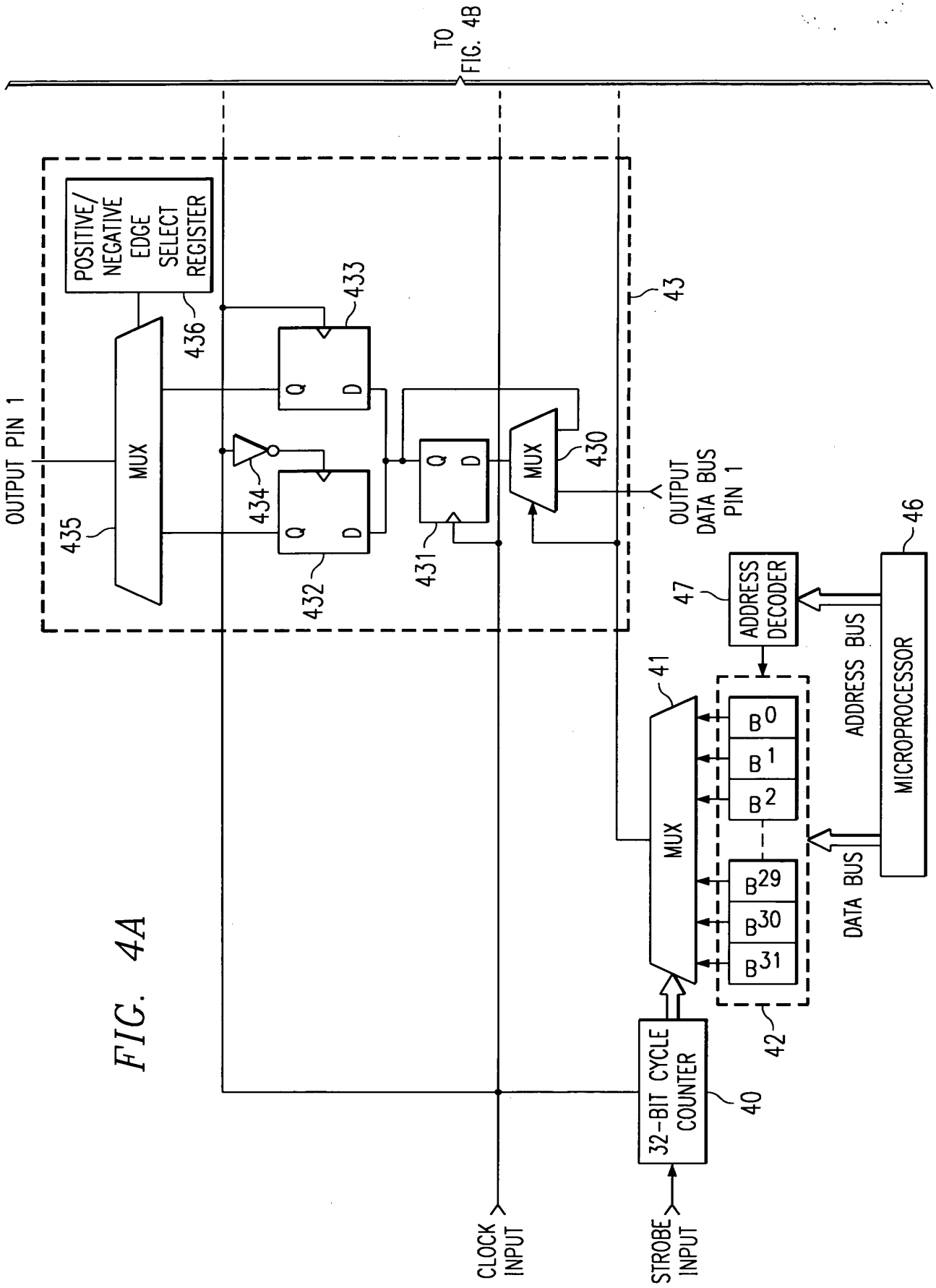

TO FIG. 4B
POSITIVE/ NEGATIVE EDGE SELECT REGISTER
436
433
43
OUTPUT PIN 1
MUX
435
434
Q
D
432
431
430
OUTPUT DATA BUS PIN 1
47
ADDRESS DECODER
46
ADDRESS BUS
MICROPROCESSOR
41
B0
B1
B2
B29
B30
B31
DATA BUS
42
32-BIT CYCLE COUNTER
40
CLOCK INPUT
STROBE INPUT

FIG. 4A

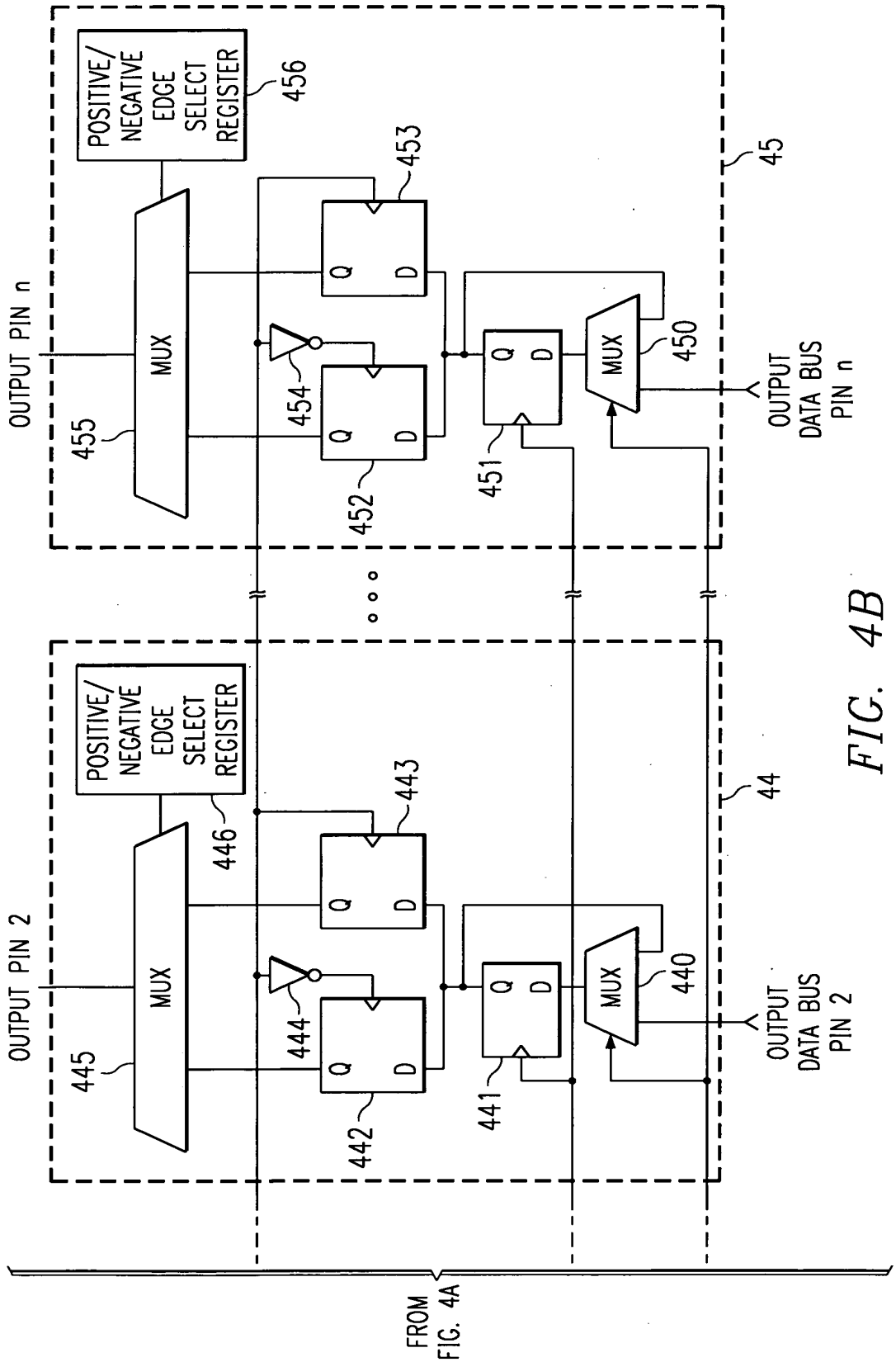

POSITIVE/ NEGATIVE EDGE SELECT REGISTER
456
453
45
OUTPUT PIN n
MUX
455
454
452
451
450
OUTPUT DATA BUS PIN n
POSITIVE/ NEGATIVE EDGE SELECT REGISTER
446
443
44
OUTPUT PIN 2
MUX
445
444
442
441
440
OUTPUT DATA BUS PIN 2
FROM FIG. 4A

FIG. 4B

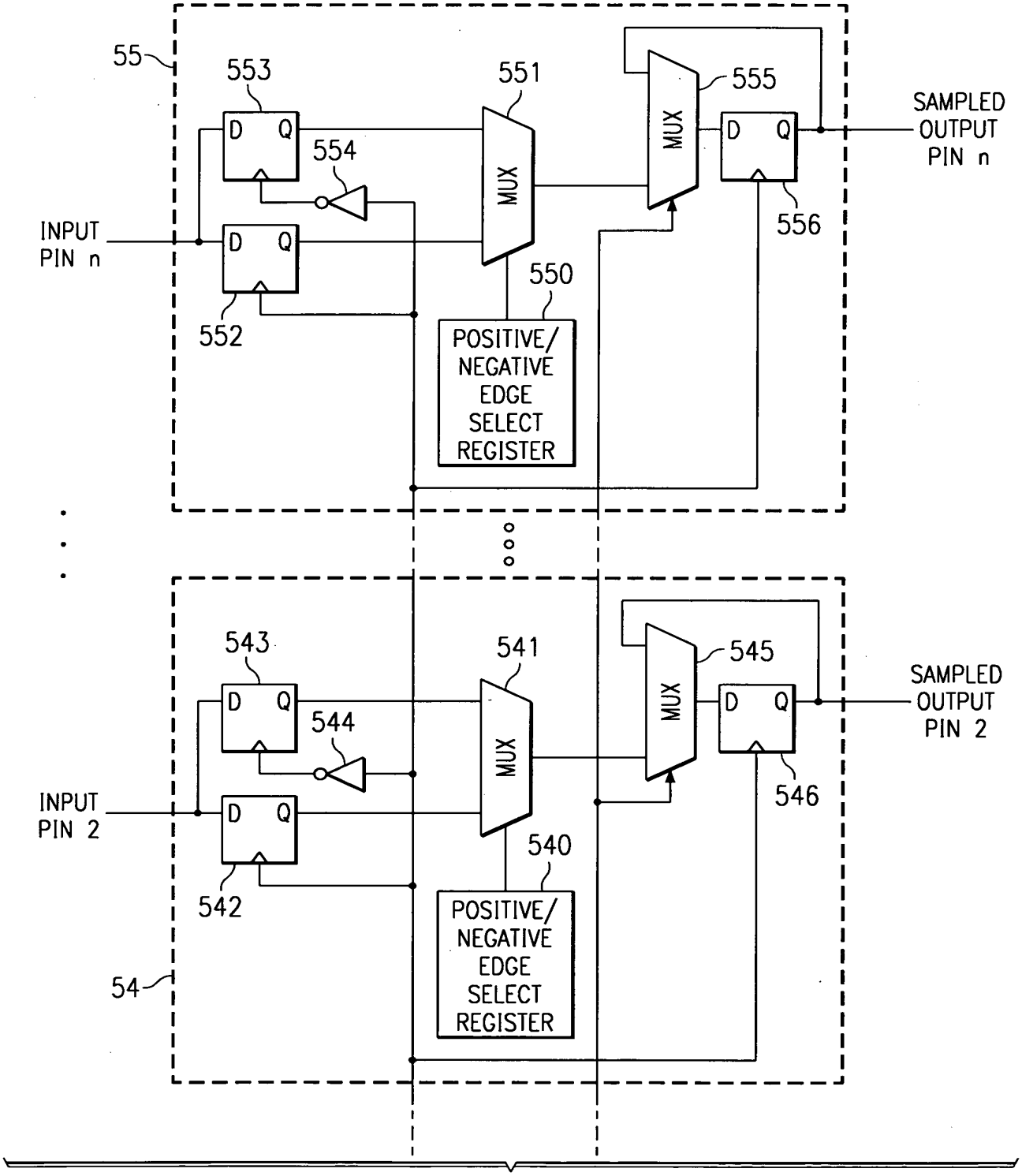

55
553
551
555
D Q
554
MUX
MUX
D Q
SAMPLED
OUTPUT
PIN n
INPUT
PIN n
D Q
556
550
552
POSITIVE/
NEGATIVE
EDGE
SELECT
REGISTER
543
541
545
D Q
544
MUX
MUX
D Q
SAMPLED
OUTPUT
PIN 2
INPUT
PIN 2
D Q
546
540
542
POSITIVE/
NEGATIVE
EDGE
SELECT
REGISTER
54
TO FIG. 5B

FIG. 5A

FIG. 5B

FROM FIG. 5A

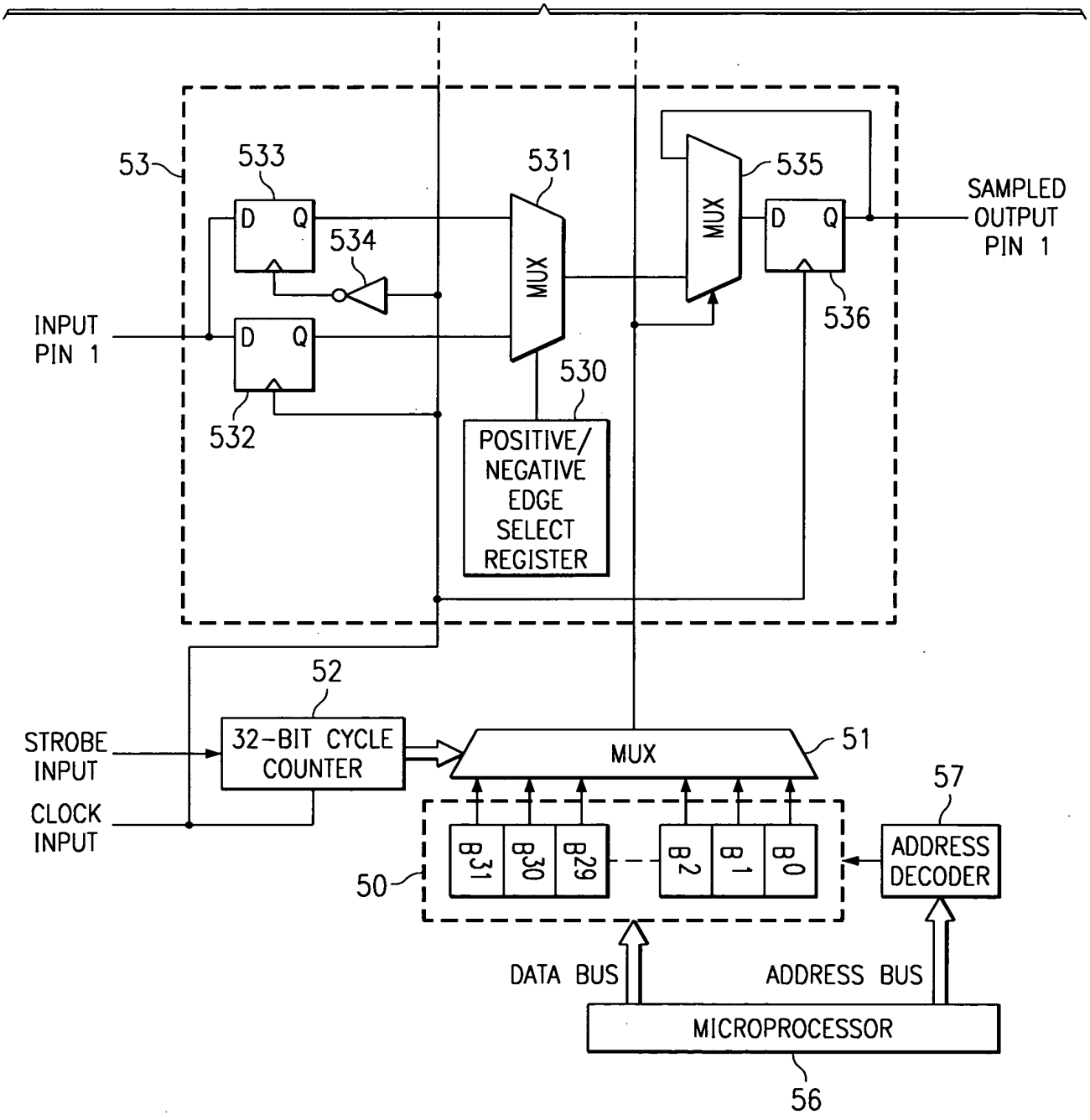


FIG. 6

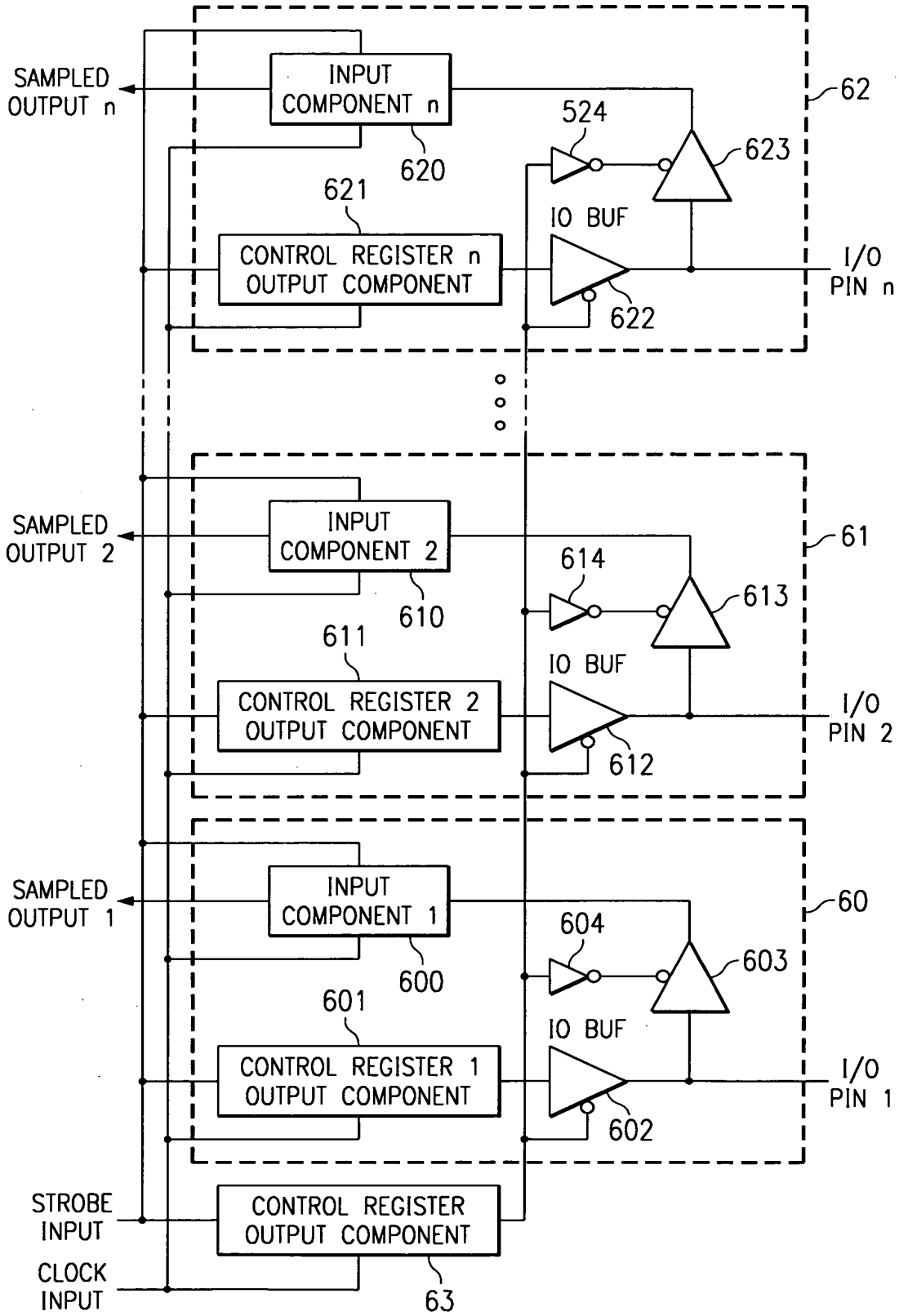
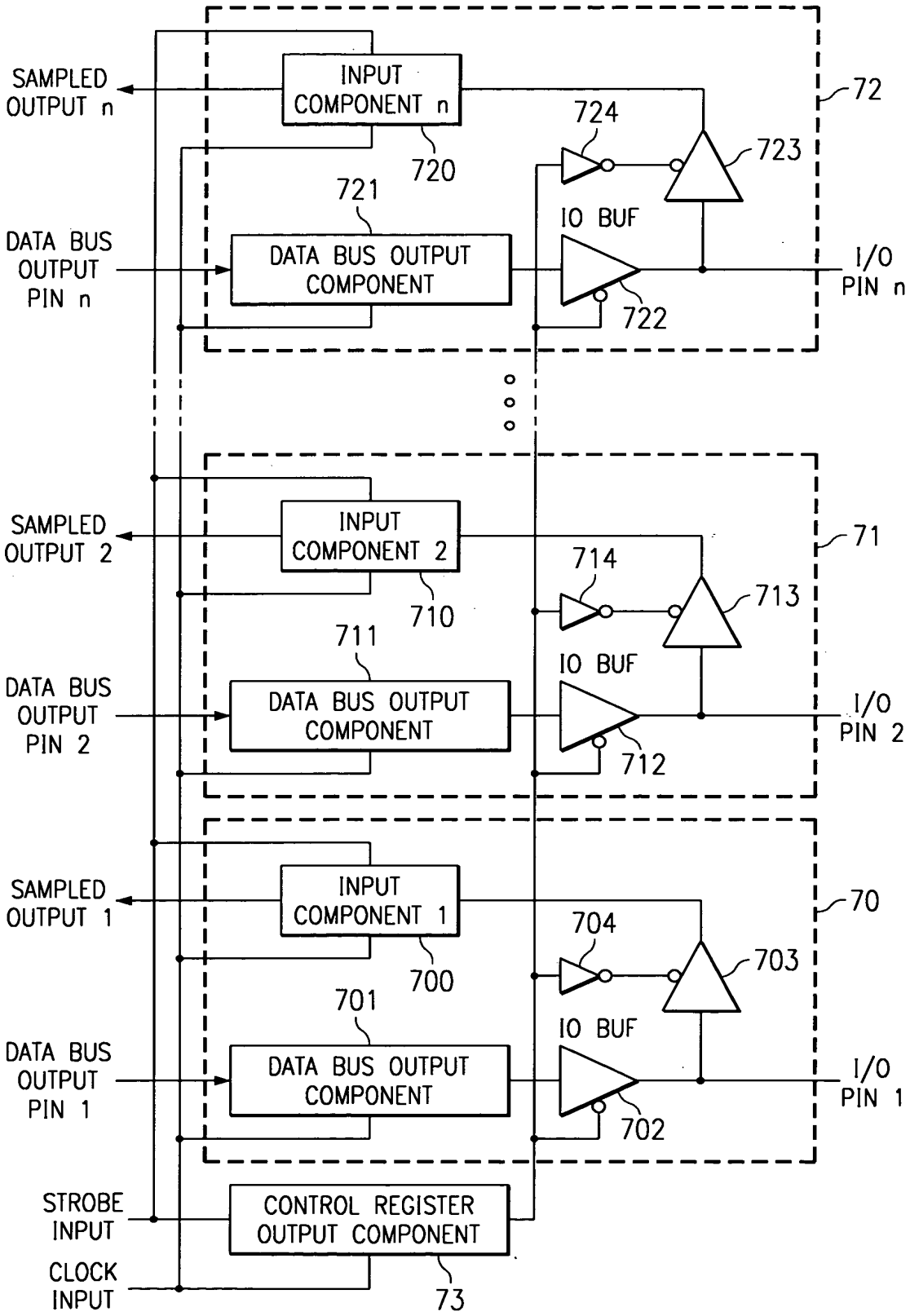

SAMPLED OUTPUT n
INPUT COMPONENT n
620
524
623
62
621
IO BUF
CONTROL REGISTER n OUTPUT COMPONENT
I/O PIN n
622
SAMPLED OUTPUT 2
INPUT COMPONENT 2
610
614
613
61
611
IO BUF
CONTROL REGISTER 2 OUTPUT COMPONENT
I/O PIN 2
612
SAMPLED OUTPUT 1
INPUT COMPONENT 1
600
604
603
60
601
IO BUF
CONTROL REGISTER 1 OUTPUT COMPONENT
I/O PIN 1
602
STROBE INPUT
CLOCK INPUT
CONTROL REGISTER OUTPUT COMPONENT
63

FIG. 7


SAMPLED OUTPUT n
INPUT COMPONENT n
720
724
723
72
721
DATA BUS OUTPUT PIN n
DATA BUS OUTPUT COMPONENT
IO BUF
722
I/O PIN n
SAMPLED OUTPUT 2
INPUT COMPONENT 2
710
714
713
71
711
DATA BUS OUTPUT PIN 2
DATA BUS OUTPUT COMPONENT
IO BUF
712
I/O PIN 2
SAMPLED OUTPUT 1
INPUT COMPONENT 1
700
704
703
70
701
DATA BUS OUTPUT PIN 1
DATA BUS OUTPUT COMPONENT
IO BUF
702
I/O PIN 1
STROBE INPUT
CLOCK INPUT
CONTROL REGISTER OUTPUT COMPONENT
73